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Hybrid intelligent system for a synchronous rectifier converter control and soft switching ensurement

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ABSTRACT

This research implements an intelligent control strategy in a synchronous rectifier buck converter to assure that the converter operates in soft-switching mode. The converter is analysed and the two different switching modes are presented: Hard-switching and Soft-Switching. Afterwards, an intelligent model is implemented with the aim of identifying and classifying the switching mode of the power converter. The model implementation is based on classification methods through intelligent algorithms that differentiate between the two modes of operation. Satisfactory results have been obtained with the implemented classification method, achieving high accuracy and allowing the implementation of the model into the control strategy of the converter; assuring that the converter operates in the desired operating mode: Soft-Switching mode.

1. Introduction

In the last years, the power electronics has became one of the main fields in the electronic industry. The power converters are in every device that we use, from a cell phone to the car we drive everyday to work; they are the basis of the electric supply of appliances and industrial equipment. With the introduction of the electric vehicles and the current trend of the renewable energy, the industry requires improvements in this field of knowledge, therefore, many researches are happening in this area. Nowadays, most of the researches are not focusing in the introduction of new topologies but on the improvement and optimization of them, finding new applications, new materials, increasing the efficiency, etc [1,2]. Thus, even large international companies, such as Google, are forcing and pushing the research and development of new technologies and designs through awards in order to optimize current devices [3].

As shown in [1,2,4–6], many institutes are researching with the aim of improving already known power converters by modifying the control strategies, substituting the transistors technologies (using wide band-gap materials), etc. In many of the researches, the main aim is reducing the power losses and obtaining the smallest design, which means the most efficient design that allows using cooling system and delivering the maximum possible power.

With this aim of increasing the efficiency, thus lowering the power losses, different topologies of power converters can be used. One of the main changes that have been introduced to reduce the losses is substituting the diodes by transistors, lowering in this way the conduction losses and avoiding the turn-on voltage of the diode. Specially with low voltage applications this change has a big effect, as the turn-on voltage is not present [7]. One improvement is the use of topologies based on resonant circuits, reducing the switching losses practically to zero. The switching can be lossless when one of these two conditions happens: during the commutation of the transistors the current is brought to 0 or that the voltage across the switching device is also worth 0 at that particular moment. These conditions are achieved thanks to the resonance of different components in the power converter, which are capacitors and coils/transformers (or parasitics of both). As an example, in the LLC (inductor-inductor-capacitor) resonant converter the resonance happens between the resonance capacitor, resonance inductor and the transformer inductance [8]. In other cases, though it is not possible to achieve the condition of 0 current or 0 voltage, it is still possible to decrease the voltage to a certain value. In this case, the converter switches when the voltage is at a valley, avoiding in this way to switch with the full-voltage. They are the so-called quasi-resonant converters, as for example in the flyback type converter [9].

Moreover, in the last years new materials have been introduced in the field of power electronics: the wide band-gap materials. They are the Silicon Carbide (SiC) and Gallium Nitride (GaN). Both

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of them have better characteristics that can be applied in this field, such as higher switching speeds, higher voltage withstand, better thermal conductivity, lower on-state resistance, etc. Therefore, these materials are a good chance to increase the efficiency and reduce the size of power converters. Nowadays, because of the already mentioned benefits and the reduction of production costs in the last years, the Silicon Carbide (SiC) and Gallium Nitride (GaN) are already replacing Silicon power devices in the power converters [2]. Furthermore, with the introduction of these new materials, the use of some techniques to achieve Soft-switching become more attractive due to the better characteristics of the transistors [3].

A comparison of different methods to achieve SS in a buck converter are described in the Table 1.

Furthermore, Artificial Intelligence (AI) is expanding rapidly in the every research areas, developing systems with intelligence capable of learning as humans. The power electronics field is also being influenced by the AI, providing solutions in many applications [16]. In the design of components, like in [17,18], the AI is used in the design of inductors, improving traditional methods of development and providing accurate results compared with the measured prototypes. In [19–21], the authors proposed a intelligent control system based on Artificial Intelligence by implementing the algorithm into the embedded controller, improving in this way the system autonomy. In [19,21] the algorithm are used to extract the maximum energy from renewable energy systems such as wind turbines or solar panels, tracking the maximum power in real time. Most of the machine learning algorithms are based on Multilayer Perceptron as it provides high performance and very high accuracy.

The Artificial Intelligence is getting more and more into this area of knowledge, helping the developers and engineers to design the power converters with the most suitable components, achieving higher efficiencies.

This document is structured as follows: first, the case study is presented; analysing and describing the converter used in this research. Then, the different operation modes of the buck converter are defined, distinguishing between Hard- and Soft-switching modes. Afterwards, the control scheme is also explained in Section 2. The Section 3 describes the used intelligent techniques to identify the operation mode and how the model is created. In Section 4 the used of the model approach in the power converter is described. Then, in Section 5, the accuracy of the algorithm to classify the operating modes is presented and finally the conclusions and future works are drawn, in Section 6.

2. Case study

In this section the case of study is presented. This section is divided into 4 different subsections to provide a more comprehensive and easy explanation. In the first part, the converter that is used in this research is presented. Then follows the controller of the converter, explaining the voltage control, the peak current control and the proportional-integral-derivative (PID) controller used in both cases. Afterwards, the difference between Hard-switching (HS) and Soft-switching (SS) is explained in reference to this converter. Finally, the simulation of the power converter used in this research is presented.

2.1. Synchronous rectifier buck converter

In this research, a buck converter with a synchronous rectifier topology is analyzed. The Fig. 1 shows the converter used in this research. This topology has been selected as it is one of the most simply and most used: the half-bridge is the base component of many power circuits, as buck, boost, full-bridge, etc. This converter can be divided into 3 main parts: the input filter, represented in the Fig. 1 by the input capacitor (Cin), the switching components, in this case T1 and T2, and the output filter, made by an inductor and a capacitor (L and Cout).

Traditionally, the buck converter had a controlled switch (T1), like a MOSFET, and a non-controlled switch, a diode. In this case, the implementation of the second switch (T2), allows a reduction of the losses in the converter, avoiding the on-state voltage of the diode and providing better control of the output, specially at lower voltages. In this way, the forward voltage of the diode is not present anymore and the losses depends just on the on-resistance of the low side switch. Both switches work complementary to each other: if the high-side switch (T1) is turned-on, the low-side switch is blocking the voltage and vice versa. The connection node between the components is the switching node (Vsw), in this node the voltage is pulsed and jumping between Vin, when T1 is conducting, and ground (0 V), when T2 is conducting. The voltage pulses with a certain frequency, called switching frequency, and the time when the high-side switch is on (Vsw = Vin) with respect to the period of the switching frequency is called duty cycle. The output voltage of the buck converter is proportional to the input voltage and the duty cycle.

The output filter, inductor-capacitor filter, is connected at the switching node and it is used to filter the high frequency pulsed voltage, storing energy in the inductor and capacitor to provide a constant output and eliminating the noise generated by the switches.

The Fig. 2 shows a representation of the switching transition through the high-side switch of the converter. At the beginning, the transistor is blocking the applied voltage. Then, when the transition starts, a conducting channel is formed in the device, allowing the current to start flowing. At the same time, the voltage across the device drops while the current increase until the transistor is completely turned-on. In this instant, the losses are determined

Table 1
Comparison of different methods to achieve SS in a buck converter.

Category	Fundamentals	Advantages	Drawbacks	Ref.
Resonance circuit	Addition of a resonance tank that provides the ZVS condition	Achieve resonance of high-side switch with fixed frequency control and low inductor ripple	Additional resonance circuit: inductor and capacitor	[10] [11] [12]
Auxiliary circuit with coupled inductors	New circuit topology with additional couple inductors and diode	Easy control as it uses fixed frequency and the auxiliary		
circuit uses a diode	Additional coupled inductors and diode	[13]		
Auxiliary circuit with switches	Additional switch in parallel to the inductor to provide an auxiliary path for the current	Achieve resonance by providing a current path	Additional double switch and control circuit	[14] [15]
Authors proposal	Basic buck topology with intelligent model to assure SS operation	No additional components are needed and relies on control	Harder control implementation and variable frequency	

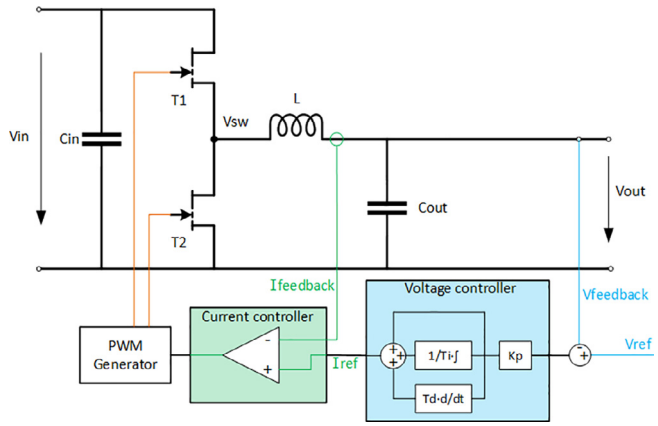


Fig. 1. Buck converter using the synchronous rectifier topology.

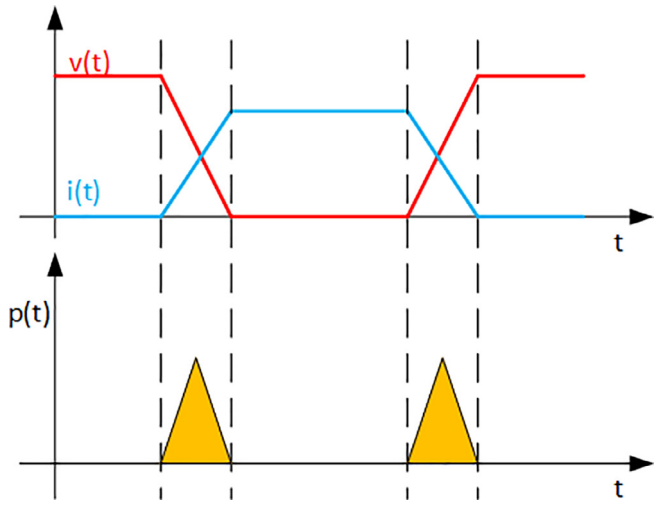


Fig. 2. Hard-switching commutation.

by the on-state resistance of the channel and the current flowing across the device.

On the other hand, when the transistor is turning-off, the conduction channel starts closing and increasing the impedance, limiting in this way the current flow. When the channel is completely closed, the device is blocking again the voltage and no current is flowing through the device.

These two transitions, turn-on and -off commutations, cause the switching losses, which in addition to the conduction losses, are the main cause of the losses in power transistors.

Moreover, the inductor is design with the aim of filtering the pulsed voltage. The selection of the right value is done accordingly to the Eq. 1. Traditionally, the design was done with the aim of keeping the ripple current low, between 5 % and the 20 % of the output current.

$$L = \frac{(V_{in} - V_{out}) \cdot D}{f \cdot I_{ripple}} \tag{1}$$

where L is the inductance value, V_{in} is the input voltage, V_{out} is the output voltage, D is the duty cycle, f is the switching frequency and I_{ripple} is the ripple current at the inductor.

2.2. Controller

The converter is usually used to provide a desired constant output voltage, thus a regulation of the output is needed. A common way to control this converter is using a proportional-integrator-derivative (PID) controller. The controller takes the measured output voltage generated by the converter and compares this value with a certain value called set-point, which is defined by the user. The obtained value is called error.

Then, the error is multiplied by a proportional constant. Also, the error is integrated over time and derived. The output of the controller is obtained by the sum of the three parts. Finally, this value is used to actuate the control signal for the switches of the power converter. The Eq. 2 shows the expression of the PID controller.

$$u_t = K_p \cdot \left[e(t) + \frac{1}{T_i} \int e(t)dt + T_d \frac{e(t)}{dt} \right] \tag{2}$$

where $u(t)$ is the control signal, $e(t)$ is the error signal which is obtained from the difference between the set-point and the measured output of the system. The parameters of the controller are: K_p, proportional gain, T_i, integral gain, and T_d, derivative gain.

The Fig. 1 shows the controller used to regulate the output voltage of the converter. As it can be seen, a cascade-controller is used, the output voltage is controlled and gives the input to the current-peak controller. The voltage regulation is done with a PID controller. The outer controller regulates the output voltage while the inner controller, which reacts faster, regulates the inductance current.

2.2.1. Voltage controller

The voltage controller is the main regulator of the system. The output voltage is measured and compared to the desired set-point defined by the user.

In the Fig. 1, the voltage controller is represented in blue.

2.2.2. Current controller

In addition to the previous PID controller used to ensure the desired output voltage, an current-peak control is added in cascade. This cascade controller sets the voltage as explained before and the control signal from previous controller is fed to the current-peak controller.

This controller takes the measured current in the inductor as control signal and compares it with the output of the voltage regulator.

2.2.3. PWM generator

As part of the controller circuit, there is a PWM generator. The aim of this part is to convert the output signal from the controller to a PWM signal. This signal is used turn-on and -off the transistors.

In this research, this is done with a “Set/Reset Flip-Flop”: when the current-peak reaches the value obtained from the voltage controller the comparator triggers its output and the gate signal of the high-side switch is set to low and the low-side switch is set to high. On the other hand, the reset happens when the clock signal that controls the switching frequency triggers the flip-flop reset.

2.3. Hard- and soft-switching modes

The switching mode explained in the previous Section ?? is the so-called Hard-switching (HS) mode, as shown in Fig. 2.

The other operation mode in which the converter can operate is the Soft-Switching (SS) mode. As shown in the Fig. 3, the voltage drops down to zero before the current starts rising; this is called

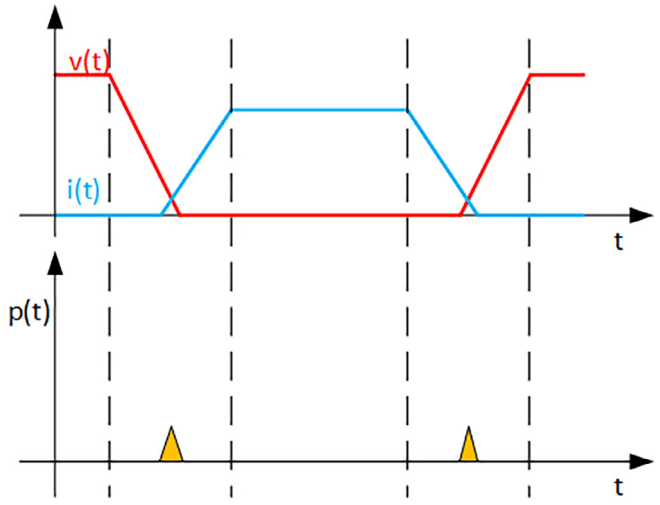


Fig. 3. Soft-switching commutation.

zero-voltage switching (ZVS). Other possibility to achieve SS happens when the current drops to zero before the voltage starts rising; in this case, the switching mode is called zero-current switching (ZCS).

In any of the previous cases, either the voltage or the current decrease to zero before the switching transition starts happening, both could happen during turn-on or turn-off commutations.

These conditions, ZCS or ZVS, are obtained thanks to resonant components placed in the power circuit, like snubber capacitors, resonance LC tanks, etc.

The boundary between the two operation modes happens when the current/voltage in ZCS/ZVS is close to 0A/0 V. In this way, the losses drops from some kilowatt peak in that moment to some few watts.

Using Soft-Switching operation mode allows decreasing the switching losses, as the current or voltage is shift during the commutation, reducing in this way the dissipated power at that instant: $P(t) = v(t) \cdot i(t)$.

In this power converter the resonance happens between the filter inductance and the parasitic output capacitance of the transistor (*Coss*), acting as a non-disipative snubber, discharging the transistor's channel before the commutation happens and making the circuit to operate in Soft-switching mode [22].

Due to the emergence of new materials for the transistors, like GaN and SiC, this way of switching takes more importance thanks to the better characteristics of those materials.

For many years, the dimensioning of the filter inductor was done to achieve low ripple current. Nowadays, the high ripple and the triangular current mode (TCM) [3,1] can be beneficial to increase the efficiency of the power converters.

Therefore, the selection of the inductor influences the efficiency of the converter. In the Fig. 4, the current ripple is shown: if the inductance is high, the current ripple can be kept low; moreover, if the value is kept low, the current ripple is very high, even crossing zero current, thus allowing Soft-Switching of the transistor and reducing the switching losses.

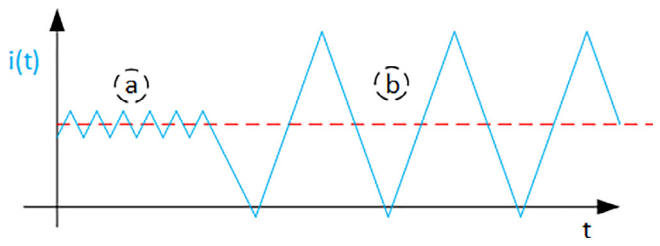


Fig. 4. Current ripple in the inductor for different frequencies.

2.4. Simulated circuit

The Fig. 5 shows the simulated circuit used in this research to study the operation of the synchronous rectifier buck converter. As simulation tool, LTSpice has been used. The components used in the simulation are default ones, with the exception of the transistors. The transistors are simulation models obtained from a manufacturer, in this case GaN Systems [23], and they represent the behavioral model of the device.

Furthermore, the other components used in the simulations are:

- Input source: The input voltage is generated by a DC voltage source. The applied input voltage is 400 V.
- Input capacitor: Though the voltage source is ideal, a input capacitor of 10 μF is placed in front of the half-bridge with the aim of filtering the current ripple.
- Transistors: the chosen transistors are from the company GaN Systems. The manufacturer number is GS66516T [23]. They are 650 V gallium nitride devices with an on-state resistance of 25 mΩ and a current capability of 60 A.
- Gate source: The gate source is simulated by an ideal voltage source that generates a square signal. The applied voltage varies from 0 to 5 V, the duty cycle is set to 50 % and the switching frequency is varied to achieve Hard- or Soft-switching. The chosen values for the switching frequency vary from 80 kHz to 2 MHz.
- Gate resistor: With the aim of limiting the peak current when switching, a gate resistor of 10 Ω is placed at the gate.
- Inductor: the inductor value is chosen accordingly to the Eq. 1, considering the previous values and assuming the ripple to be either 20 % at Hard-switching mode or 200 % at Soft-switching mode, to allow the ZCS. in this case, the chosen inductor is 25μH.
- Output capacitor: its value has been defined to filter the output voltage and provide stability to the circuit. In this case, the chosen value is 2 μF.
- Load: the output load is a resistor, which value is varied from 10 to 100 Ω. The variation of the load provides different operation points to obtain the dataset.

In addition to the power converter, the controller has been added. In this case, an analog controller is added to the simulation and it is composed by 2 different parts, the voltage controller and the current peak controller.

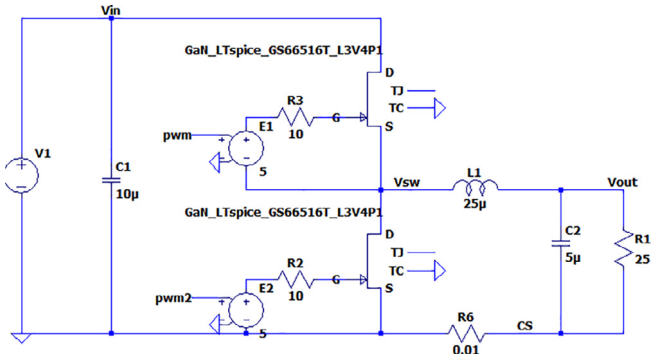


Fig. 5. Simulated synchronous rectifier buck converter.

The voltage controller is shown in the Fig. 6, where the components are used to implement the PID expression of the Eq. 2.

On the other hand, the peak-current controller is shown in the Fig. 7.

The last element shown in the Fig. 7 is the PWM generator, that generates a PWM signal at a fixed frequency.

The simulation of the circuit have been done as explained above. In total, 80 different simulation have been done, varying from HS and SS mode. The load is varied from 10 to 100 Ohm and the switching frequency as the peak-current are varied accordingly to the operation mode. When the converter is used in HS mode, the ripple of the current is defined to be 20 % and when the converter is operated in SS mode, the current ripple is set to 200 %.

3. Hybrid intelligent model

With the aim of classifying in which operating mode the power converter is working, a hybrid intelligent model have been implemented. Four different algorithms have been tested to the data-set obtained from simulation results.

The Fig. 8 presents the model approach that is followed in this research: the obtained data-set from simulation is the input to the model; then, this data is pre-processed to obtain more representative parameters for the operating mode detection. Afterwards, the data is separated into different clusters and the four classification algorithms are applied.

3.1. Data-set

As mentioned above, the data-set is obtained from simulation using the LTSpice simulation tool. The proposed power converter has been simulated at both working modes and varying the output load for a certain output voltage. With the aim of having a consistent data, the circuit is kept unchanged during the whole recompilation of data.

Forty simulation runs have been done for the converter operating in HS, same with the converter operating in SS mode, obtaining a balanced data-set.

The following variables are measured during the simulation:

- Input voltage: the converter input voltage is 400 V.
- Output voltage: is controlled at 200 V, with a voltage ripple of 5%.
- Switching node voltage (*Vsw*): this voltage is measured at the node Vsw shown in the Fig. 5). The voltage in this point varies as a pulsed signal from 0 up to 400 V, varying the frequency from 0.08 – 2 MHz.

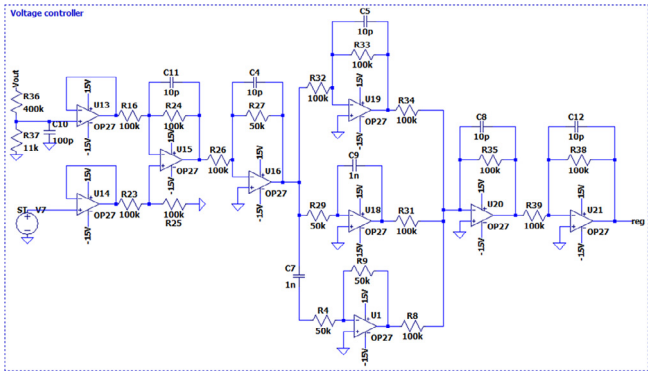


Fig. 6. Voltage controller of the converter.

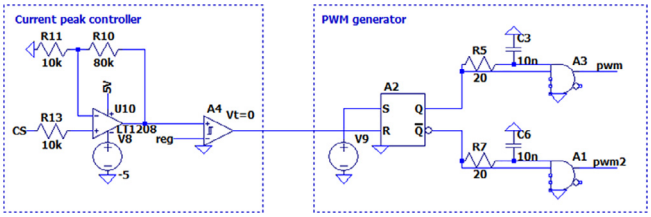


Fig. 7. Peak-current controller of the converter and PWM generator.

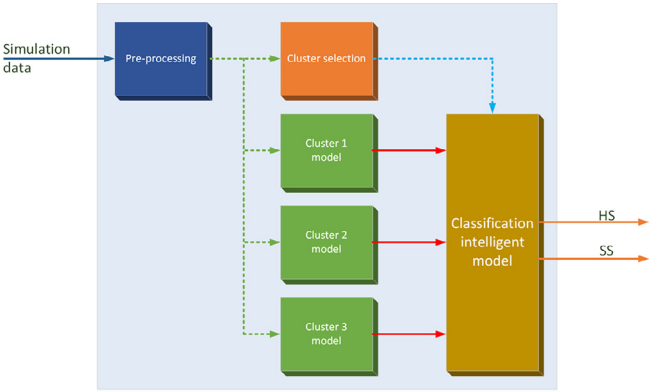


Fig. 8. Model approach.

- Current at the inductor: the shape of the ripple current is triangular. It varies depending on the output load and the switching frequency. In HS, as in the Fig. 9a, the current varies at a maximum ripple of 20 % of the average current while in SS, as in the Fig. 9b, the current drops down to 0 A, meaning that the ripple is 200 % of the output current.
- Output current: that flows through the load.

The Fig. 9a shows a graph with 3 of the 5 imported variables where the converter operates in HS mode: the voltage at the switching node in blue, the current at the inductor in red and the output voltage at the load in green. In a similar manner, the Fig. 9b shows the same but the converter is operating in SS mode. As it can be seen, the current ripple drops down to 0A in the SS mode while in HS the ripple is kept smaller.

Moreover, in both Figs. 9a and 9b, the losses of the high-side switch are represented. The peak value is reduced from almost 17 kW down to less than 3 kW, representing the SS condition.

With the aim of determining the power loss on the switching transistor, a comparison between HS and SS mode is carried out.

As explained previously, in HS mode, the current ripple is kept to 20% of the average output current while in SS, the ripple is 220%. Considering then a switching frequency of 500 kHz, a load current of 8A and the used transistor are the GS66516T [23].The output capacitance used in the calculation is the "Effective Output Capacitance VDS = 0 to 400 V Time Related"

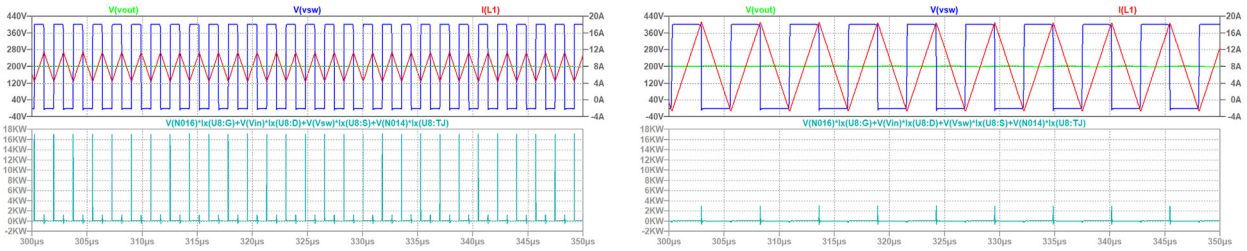
The losses calculations results in:

Hard-switching mode:

- Conduction losses:

$$I_{rms} = \sqrt{I_{avg}^2 + \left(\frac{I_{pk}}{\sqrt{3}}\right)^2} = \sqrt{(8A)^2 + \left(\frac{10\% \cdot 8A}{\sqrt{3}}\right)^2} = 8,01A \quad (3)$$

$$P_{cond} = I_{rms}^2 \cdot R_{on} = 8,01A^2 \cdot 32m\Omega = 2,054W \quad (4)$$



(a) Simulation results of synchronous rectifier buck converter in HS mode.

(b) Simulation results of synchronous rectifier buck converter in SS mode.

Fig. 9. Losses comparison between HS and SS mode.

- Switching losses:

$$P_{Coss} = \frac{1}{2} C_{oss} \cdot f_{sw} \cdot V^2 = 0.5 \cdot 335pF \cdot 500kHz \cdot 400V^2 = 13,4W \quad (5)$$

$$P_{VI} = \frac{1}{2} V \cdot I_{avg} \cdot t_r \cdot f_{sw} = 0.5 \cdot 400V \cdot 8A \cdot 12,4ns \cdot 500kHz = 9,92W \quad (6)$$

$$P_{sw} = P_{Coss} + P_{VI} = 13,4 + 9,92 = 23,32W \quad (7)$$

Soft-switching mode:

- Conduction losses:

$$I_{rms} = \sqrt{I_{avg}^2 + \left(\frac{I_{pk}}{\sqrt{3}}\right)^2} = \sqrt{(8A)^2 + \left(\frac{110\% \cdot 8A}{\sqrt{3}}\right)^2} = 9,47A \quad (8)$$

$$P_{cond} = I_{rms}^2 \cdot R_{on} = 9,47A^2 \cdot 32m\Omega = 2,87W \quad (9)$$

- Switching losses:

$$P_{sw} = \frac{1}{2} C_{oss} \cdot f_{sw} \cdot V^2 = 0.5 \cdot 335pF \cdot 500kHz \cdot 4V^2 = 1,34mW \quad (10)$$

$$P_{VI} = \frac{1}{2} V \cdot I_{avg} \cdot t_r \cdot f_{sw} = 0.5 \cdot 4V \cdot (-1A) \cdot 12,4ns \cdot 500kHz = 12,4mW \quad (11)$$

$$P_{sw} = P_{Coss} + P_{VI} = 1,34mW + 12,4mW = 13,74mW \quad (12)$$

As it can be seen, the losses reduction are by a factor of $25,37W$ / $2,88W$ = $8,78$ in this case. If the switching frequency rises, the reduction achieved can be further.

Moreover, with the aim of clarifying the loss reduction, the Fig. 9 shows the losses on the transistors in HS and SS mode.

From these simulated variables, the final data-set to build the model has been created, calculating new useful variables from the explained above.

From previous described signals, the switching node voltage has special relevance as it reflects how the commutation happens.

This signal is analyzed, *Vsw*, and the first and second derivative are applied to it. In this manner, the derivative of the on- and off-states are 0, so that part of the data can be removed, keeping the remaining information of the transitions.

Then, assuming that the rising and falling of the signal *Vsw* happens between the 5% and 95% of the input voltage, those edges can be easily separated. In the Fig. 10 the representation of how the edges are separated is shown. They provide information of how the transition occurs. Also, from that Fig. 10, the commutation times can be obtained, being *tr* the rise time and *tf* the fall time.

Moreover, as previously, the first and second derivative is applied to the rising and falling edge signals.

If the integral is calculated, the area *ar* under the rising signal is obtained and the same for the falling signal, *af*. Those areas provides lot of information of the commutation.

From the previous analysis, 8 signals are obtained from *Vsw*:

- Raw data: shown as the red signal in the Fig. 10.
- First derivative of the raw data.
- Second derivative of the raw data.
- Rising and falling edge data: shown as dotted blue signal in the Fig. 10.
- First derivative of the rising and falling edge signal.
- Second derivative of the rising and falling edge signal.
- Integral of the rising edge signal: area *ar* in the Fig. 10
- Integral of the falling edge signal: area *af* in the Fig. 10

With the aim of obtaining further information, the statistics in the Table 2 have been applied to the previous 8 variables. Obtaining a matrix of size 8x6 for each of the simulation results.

3.2. Methods

The different techniques used to implement the hybrid models are the following: These methods are described bellow.

3.2.1. Data clustering. The K-Means algorithm.

First step is to separate the data into groups or clusters through an unsupervised technique. The proposed algorithm is K-Means, which creates clusters of data with similar characteristics [24,25]. The initial data, *x* is compared with the rest by means of

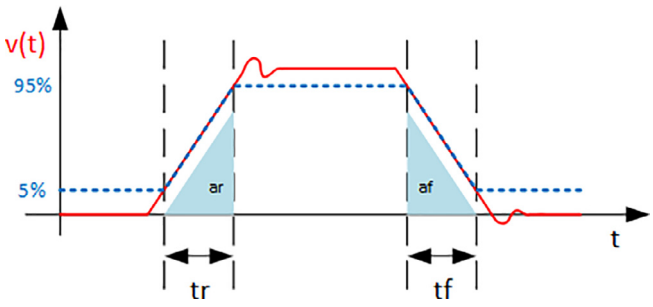


Fig. 10. Rising and falling edge of the switching node voltage, in dashed blue, and the original signal in continuous red.

Table 2
Summary of dataset variables.

Signals	Operations applied to each signal
Raw data Vsw	
1st derivative from raw data	Average
2nd derivative from raw data	Standard deviation
Rising/falling edge data	Variance
1st derivative rising/falling edge data	Co-variance
2nd derivative rising/falling edge data	RMS
Rising edge integral	THD
Falling edge integral	

distance between the samples and the centroids. The centroids are defined as the geometrical center of the group/cluster.

During the training of the algorithm, the centroids are chosen and calculated. To do so, first they are defined randomly from the initial data and, then, based on the distance of the samples, the data is classified; the closer the sample to the centroid is, the better. Once this process has finished for the complete data-set, the centroids are recalculated for each group. For every iteration, the centroids may change and the process is considered finished when the position of the centroids keep unchanged for 2 consecutive iterations.

3.2.2. Multilayer perceptron

The used artificial neural network in this research is the perceptron, which emulates the brain. This algorithm is made up of a single hidden layer, but when the number of layers increase, then it is called multilayer perceptron. The structure follows by an input and an output layer with the multiple hidden layer in between. The hidden layers process the activation function. The connection between the layers is done with weighted connections, which are adjusted to decrease the error of the output [19].

3.2.3. Linear discrimination analysis

The Linear Discrimination Analysis, L.D.A., is a algorithm that reduces the dimension of the input data, projects the data from a high- to a low-dimensional space and, then, does the classification in the lower dimensional space. As shown in Eq. 13, the algorithm uses a weight vector W to increase the separation between the samples, E, and reducing the separation of the similar samples [26]. The classification achieves good results when the projections of the class involves exposing long distance along the direction of vector W.

$$P_i = W^T E_i \tag{13}$$

The projections are calculated as in Eq. 14.

$$\mu_1 - \mu_2 = W^T(m_1 - m_2) \tag{14}$$

where $(m_1 - m_2$ represents the mean vector of the two classes.

This classification technique provides 2 outputs: a binary decision obtained from a gradual decision. The projection done by the algorithm can be interpreted as a measurement of the distance between the samples of each class, maximising the ratio between the inter-class variance to the intra-class variance. When this distance between the data is higher, the achieve performance is as well higher [27].

3.2.4. Support vector machine

The Support Vector Machine, S.V.M., is widely used as supervised classification method [28]. The function looks for two different hyper-planes of data that are separated by the maximum distance [28]. Thus, using a kernel operator to project the samples in a high dimensional space and defining training vectors near the hyperplane.

3.2.5. Ensemble

An ensemble is a combination of multiple methods to improve the accuracy achieved by one classifier [29]. They usually proceed by selecting the weak learners to obtain a regularization of the data [30].

The method tries to find a set of weights α_t that minimize the expression 15.

$$\sum_{n=1}^{N} w_n g\left(\left(\sum_{t=1}^{T}\alpha_t h_t(x_n)\right), y_n\right) + \lambda\sum_{t=1}^{T}|\alpha_t| \tag{15}$$

where,

- $\lambda \geqslant 0$ is the regularization parameter.
- h_t is a weak learner in the ensemble trained on N observations with predictors x_n, responses y_n, and weights w_n.
- $g(f, y) = (f - y)^2$ is the square error.

3.3. Classification performance

With the aim of validating and checking the proposed methods, the algorithms run the validation data and the results are compared. The performance of the classification is measured by the confusion matrix, thus measuring the quality of the used method.

The two times two matrix is as shown in the Table 3. where the columns are the true values, from the validation data, and the rows are the predicted values, from the previous classification algorithms [31].

When the true values and the predicted value are in accordance, the results are true positives or true negatives (TP or TN respectively) and when they do not coincide, they are defined as false positives and false negatives (FP or FN)[31]. hen, from the matrix, 5 different indicators describe the performance of the classification algorithms; Eqs. (16)–(20) [31].

$$SEnsitivity = \frac{TP}{(TP + FN)} \tag{16}$$

$$SPeCificity = \frac{TN}{(FP + TN)} \tag{17}$$

$$PositivePredictionValue = \frac{TP}{(TP + FP)} \tag{18}$$

$$NegativePredictionValue = \frac{TN}{(TN + FN)} \tag{19}$$

$$ACCuracy = \frac{TP + TN}{(TP + TN + FP + FN)} \tag{20}$$

3.4. Experiments description

The first experiment that has been carried out was implementing the model without clustering, providing a comparison starting point for the hybrid model.

Table 3
Example of 2x2 confusion matrix.

		True value	
		P	**N**
Predicted value	**P**	TP	FP
	N	FN	TN

With the aim of training the model, 75% of the data-set has been used. The rest of the data, 25%, is used for validation. This division is done randomly.

As described in the Section 3.2, the following algorithms have been applied:

- M.L.P.: the Levenberg–Marquardt backpropagation algorithm has been used. The number of neurons in the hidden layer varies from 1 to 10.
- L.D.A.: the regularized LDA is used as discriminant, where all classes have the same co-variance matrix.
- S.V.M.: The linear kernel function is used, as it provides the best performance in two-class learning.
- Ensemble: the adaptive logistic regression is used for binary classification. The cycles vary from 10 to 100 in steps of 10. The weak-learners used function is the decision tree.

Afterwards, with the 25% of the validation data, the algorithms are checked. The obtained predictions are compared with the verified data using the confusion matrix.

Finally, the algorithms are tested after the data has been separated into clusters, implementing in this way a hybrid model. The clustering method is K-Means, using a number of clusters from 2 up to 10. All previous classification techniques are applied to each of the clusters and the validation of the hybrid model has been done in the same manner.

4. Approach

The main contribution of this research is the definition and implementation of the approach shown in the Fig. 11.

This flow chart represents the buck converter that is controlled to operate in Soft-Switching conditions. The variables used for the intelligent classifier are measured. These variables are presented in Section 3.1, such as the voltage in the switching node or current. Then, the system classifies and determines in which operating mode the converter is working. If the converter is working in Hard-Switching, the frequency is changed and waits until the steady state is reached again. If the converter is already in SS mode, the model does not do anything.

The sequence is repeated until the system detects that the converter is in Soft-Switching mode.

This intelligent control system can interact even if there are changes on the load or any external condition of the converter, as the system is checking the operating mode continuously.

The mode is implemented into the control loop as in the Fig. 12. The Soft-switching detector is controlling the switching frequency of the converter by influencing the PWM generator. The other parts of the controller, peak-current and voltage controller keep as explained above.

4.1. Experimental setup

The experimental setup is compounded by the following hardware components:

- Microcontroller board: This board has the TMS320F280049 controller from Texas Instruments. Some of the main features of this controller are: high speed PWM module with 150 ps resolution, ADCs with 3.5 Msps, internal comparators, CLA to acellerate the control loops, etc.
- Transistors board: in this case, we use the evaluation board from Gan Systems GS-EVB-HB-66516T-RN. It already integrates the gate driving circuit.

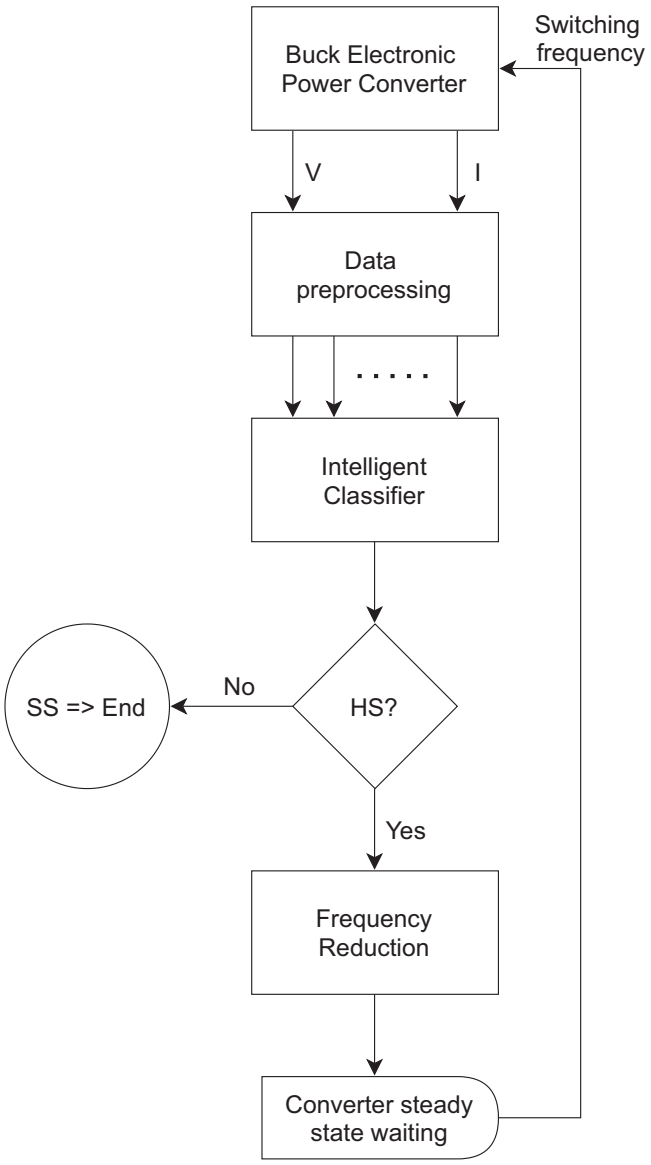


Fig. 11. Approach: Flow chart for Soft-switching control.

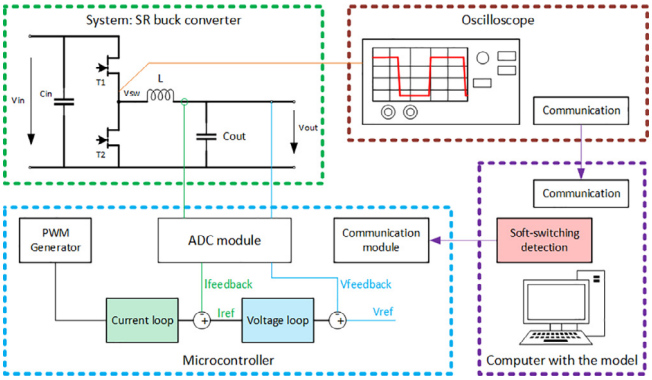


Fig. 12. Drawing of the experimental setup scheme.

- Power board: this board serve of interconnection between the microcontroller and the transistors board. In this board, the voltage and current sensing is also placed.

- Oscilloscope: The used oscilloscope is the DSO-X 3014A, which is connected to MATLAB/Simulink thanks to the Instrument Control Toolbox from MATLAB.
- Power source: the EA-PSB 9500–90 is used, to provide an input voltage of 400 V.

Moreover, the circuit parameters are the same as in the previous simulation. In Section 2.4, the description of the components and power converter details are described:

- Input voltage: is generated by a DC voltage source. The applied input voltage is 400 V.
- Input capacitor: is placed with a capacitance of 100 μF.
- Transistors: the chosen transistors are from the company GaN Systems. The manufacturer number is GS66516T [23]. They are 650 V gallium nitride devices with an on-state resistance of 25 mΩ and a current capability of 60 A.
- Gate driver circuit: the circuit to drive the transistors has been design. The gate driver used is the RAA226110 from Renesas. An signal isolator and a isolated power supply are used to provide isolation between the microcontroller and the power transistors.
- Inductor: the inductor has been design by the authors; finally using a inductance value of 25μH. The used material is 3F4 from Ferroxcube.
- Output capacitor: is selected to absorb the high ripple and with a capacitance of 10μF.
- Load: the output load is a variable. Different resistive loads as the TE type series: TE1000B22RJ.

The classification hybrid model M.L.P.1 has been used, as provides an accuracy of 100% according to the results shown with the simulation dataset.

In this work, the inductor and output voltage is measured directly by the microcontroller with the internal ADC.

As the current control is using the peak current, the PWM signal is triggered with a comparator inside the microcontroller. When the current reaches the reference voltage from the voltage control output, the PWM signal is triggered low and keeps low until the period of the signal finishes. This allows to react very fast when the peak current is detected.

Moreover, the switching node voltage measurement is done with an oscilloscope. The reason is that the rise time of the voltage is very low, in the nanoseconds range. The data is then transfered to a computer, where the model analyses the switching node data.

Finally, the output of the model is a frequency setpoint for the microcontroller. The Fig. 12 shows the experimental setup implemented.

The real hardware setup has been implemented, as shown in Fig. 13.

As previously mentioned, the current and voltage control loops are implemented in the microcontroller. Thus, in case any load variation the controller can react fast and keep the output voltage stable.

On the other hand, as the switching node voltage is a very critical and demanding measurement, due to its high rise time in the nanoseconds range, this measurement is done with an oscilloscope.

The delay between this measurement and the reaction of the model leads to some switching cycles where the converter operates in HS mode. During the time the converter is in HS mode, the losses will increase causing a temperature rise of the devices. Due to the thermal capacitance of the circuit, the temperature rise takes some time before reaching a potentially dangerous point. After few milliseconds, the SS detection model reacts and vary the switching frequency to set the converter in SS mode again; consequently, the losses are reduced and the temperature of the power module decreases back to a low level.

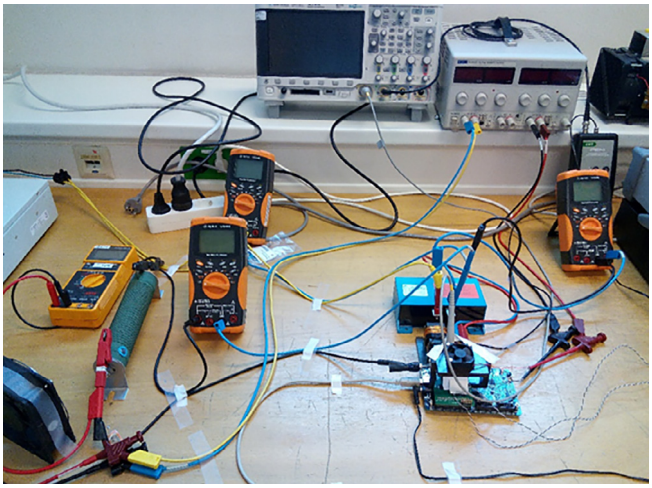


Fig. 13. Experimental setup.

The control is divided into two parts:

- Current control loop: this control loop runs inside the microcontroller. This part of the control takes care of the output current from the converter. This loop runs cycle by cycle, as it controls the peak current at the inductor.
- Voltage control loop: also runs inside the microcontroller taking care of the output voltage that the converter delivers. In this case, the loop runs every 1 ms.
- Classification model and proposed approach: this part of the control runs in a computer in the following manner: The switching node voltage is measured by an oscilloscope that sends the data to the computer via RS232. In MATLAB, the data is analysed, the operating mode is detected and the new frequency set-point is sent to the microcontroller over USB communication. The loop runs every 500 ms.

5. Results

This section presents the obtained results from the hybrid intelligent model.

The Table 4 shows the accuracy of the classification achieved with each configuration of the hybrid model. As shown there, for models with number of clusters higher than 4, the performance obtained is always of 100%.

If no clustering of the data is used, the M.L.P.7 achieves the highest accuracy, with 97.06%.

If two clusters are used, the accuracy is increased to 100%, with the models M.L.P.1 and M.L.P.5, while achieving an accuracy of 78.95% in worst case.

In Table 4, the number of clusters are indicated in the first row. Then, for each row, the obtained performance for different clusters is presented.

When the converter is checked without the presented approach, the results obtained are the shown in the Fig. 16a: the converter starts operating in SS mode, set by the user and then, with a change of the load, the converter loses this operating mode. In this figure, the output voltage (blue) as well as the inductor current (green) can be seen. The converter operates in SS mode from 0.8 ms to 1 ms, then the load increases, the controller follows the set-point but the converter moves away from the SS mode, and once this load is removed and the previous load is set again, the converter comes again into SS mode, as the current drops to 0A.

Table 4
Obtained accuracy, in percentage, for each configuration.

Clusters	1 cluster	2 cluster		3 cluster			4 cluster			
Number of cluster	1	1 of 2	2 of 2	1 of 3	2 of 3	3 of 3	1 of 4	2 of 4	3 of 4	4 of 4
M.L.P.1	81.54	100	94.74	89.47	100	100	100	100	100	100
M.L.P.2	73.53	100	94.74	100	100	100	100	100	100	100
M.L.P.3	62.26	100	94.74	100	100	100	100	100	100	100
M.L.P.4	55.88	94.74	94.74	89.47	100	100	100	100	100	100
M.L.P.5	79.41	88.89	100	100	100	100	100	100	100	100
M.L.P.6	60.29	94.73	94.74	100	100	100	100	100	100	100
M.L.P.7	97.06	94.77	94.74	89.47	100	100	100	100	100	100
M.L.P.8	73.53	94.73	94.74	100	100	100	100	100	100	100
M.L.P.9	86.76	100	94.74	100	100	100	100	100	100	100
M.L.P.10	52.94	100	94.74	100	100	100	100	100	100	100
S.V.M.	77.94	100	94.74	100	100	100	100	100	100	100
L.D.A.	60.29	100	94.74	100	100	100	100	100	100	100
Ensemble10	51.47	94.73	78.95	100	100	100	80	100	100	100
Ensem.20–100	51.47	100	78.95	100	100	100	80	100	100	100

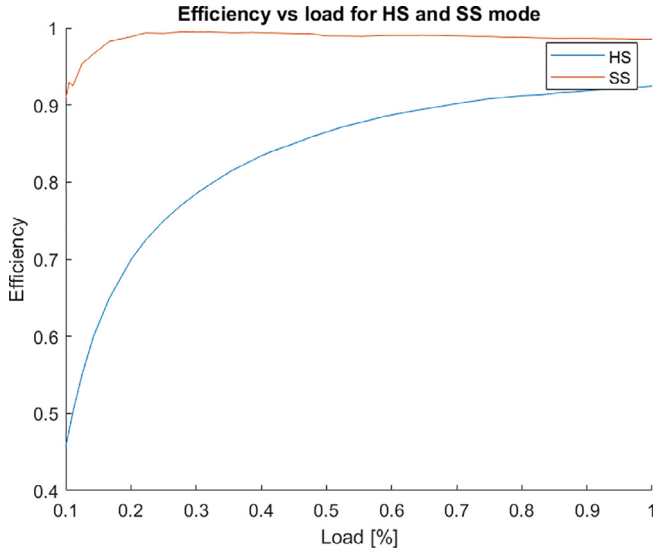


Fig. 14. Efficiency of the converter in HS and SS mode for different loads.

On the other hand, as shown in the Fig. 16b, the converter operates in SS mode with any change of load and recovers the steady-state of the voltage very fast. In this figure, the output voltage (blue) as well as the inductor current (green) can be seen. The converter operates in SS mode from 0.8 ms to 1 ms, then the load increases, and in contrast with the previous Fig. 16a, the controller follows the set-point and the converter still operates in SS mode. Also, once this load is removed and the previous load is set again, the converter continuous in SS mode.

The overall losses in the circuit without the approach are 31.71W, while in the case the approach has been implemented the losses were reduced down to 3.82W, representing a loss reduction of around 90 %.The power losses are measured, as shown in the Fig. 13 with the multimeters.

Moreover, as can be in the Fig. 13 the real setup has been implemented. As result of the real measurements, the Fig. 15 shows the converter operating in SS mode.

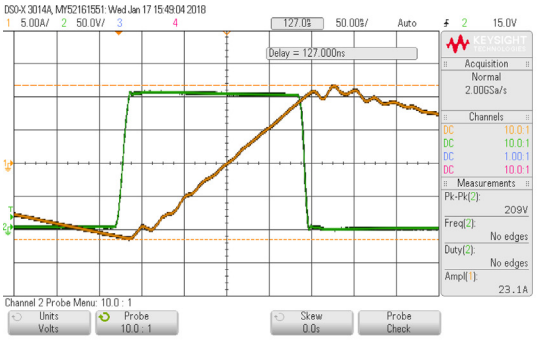
With the aim of representing the improvement of the converter efficiency with the previous characteristics, the following curve in Fig. 14 has been derived. The efficiency of the converter, either in HS or in SS mode is represented versus the applied load to the converter.

Where the current is represented as green while the yellow signal represents the voltage at the switching node. Those pictures were taken with an input voltage of 200 V, a load of 10A and switching frequency of 1Mhz.

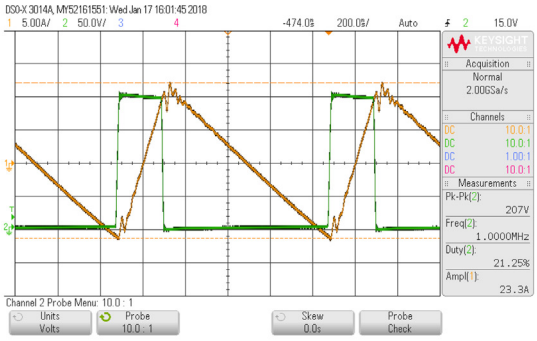
6. Conclusions and future works

In this research the implementation of a hybrid intelligent model was presented. This model is used for identifying if a power converter, in this case a buck converter, is operating in Hard-Switching or Soft-Switching mode. Afterwards, the same model is used to control the converter to operate in SS mode.

The proposed hybrid intelligent model is used to detect the operation mode of a power converter. The data-set is obtained from simulation results of the power converter and the most rele-

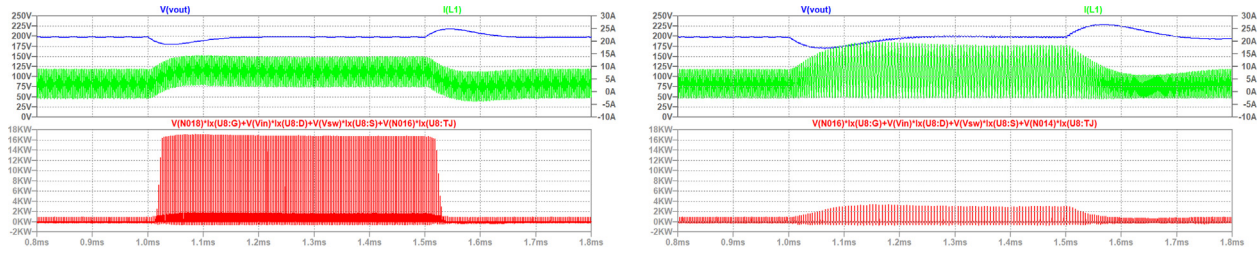


(a) Voltage and current in SS mode.



(b) Zoom of the voltage and current during commutation.

Fig. 15. Voltage (green) and current (green) in SS mode.



(a) Results without using the model approach.

(b) Results using the model approach, thus SS mode.

Fig. 16. Simulation of model approach.

vant signals are measured, 5 in this case. Afterwards, the data is pre-processed to obtain significant statistics from the data-set. The intelligent techniques are then applied to the data-set.

Finally, the model is used in the application to verify how the controller works with different loads and changes of loads.

Overall, the achieved accuracy is high, being able to detect and classify between both operating modes with 100% of accuracy.

The implementation of the hybrid intelligent model against a simple intelligent model provides an improvement of the performance, from a maximum accuracy of 97% to 100% when using 3 or more clusters. With this implementation, the efficiency of the power converter can be increased, assuring that the converter operates in the optimum working point.

The implementation of this model into the control strategy helps assuring that the converter operate with lower switching losses and the efficiency of the converter increased.

Future works will be oriented in the implementation and development of the corresponding hardware, so the hybrid intelligent model can be applied to real data from the power converter.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgement

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